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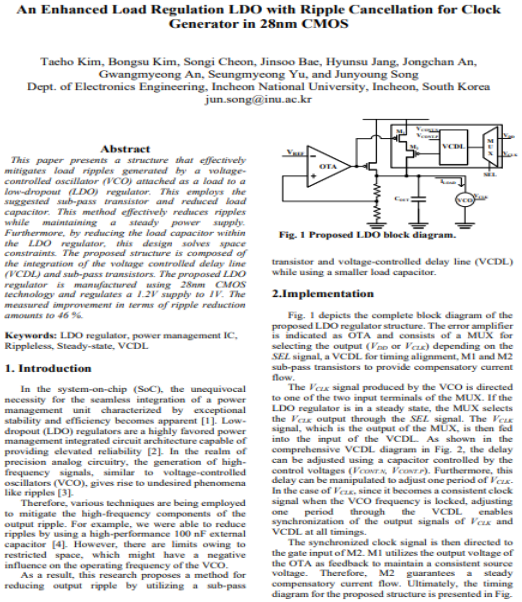
전자공학과 집적회로 및 시스템 연구실

An Enhanced Load Regulation LDO with Ripple Cancellation for Clock Generator in 28nm CMOS

Design of Low-Drop-Out Voltage Regulator

- 고속에서 동작하는 부하를 가진 LDO
- 새로운 구조의 hybrid-type LDO Regulator 설계



An Enhanced Load Regulation LDO with Ripple Cancellation for Clock Generator in 28nm CMOS

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Abstract

This paper presents a structure that effectively mitigates load ripples generated by a voltage-controlled oscillator (VCO) attached as a load to a low-dropout (LDO) regulator. This employs the suggested sub-pass transistor and reduced load capacitor. This method effectively reduces ripples while maintaining a steady power supply. Furthermore, by reducing the load capacitor within the LDO regulator, this design solves space constraints. The proposed structure is composed of the integration of the voltage controlled delay line (VCDL) and sub-pass transistors. The proposed LDO regulator is manufactured using 28nm CMOS technology and regulates a 1.2V supply to 1V. The measured improvement in terms of ripple reduction amounts to 46 %.

Keywords: LDO regulator, power management IC, Rippleless, Steady-state, VCDL

1. Introduction

In the system-on-chip (SoC), the unequivocal necessity for the seamless integration of a power management unit characterized by exceptional stability and efficiency becomes apparent [1]. Low-dropout (LDO) regulators are a highly favored power management integrated circuit architecture capable of providing elevated reliability [2]. In the realm of precision analog circuitry, the generation of high-frequency signals, similar to voltage-controlled oscillators (VCO), gives rise to undesired phenomena like ripples [3].

Therefore, various techniques are being employed to mitigate the high-frequency components of the output ripple. For example, we were able to reduce ripples by using a high-performance 100 nF external capacitor [4]. However, there are limits owing to restricted space, which might have a negative influence on the operating frequency of the VCO.

As a result, this research proposes a method for reducing output ripple by utilizing a sub-pass

Fig. 1 Proposed LDO block diagram.

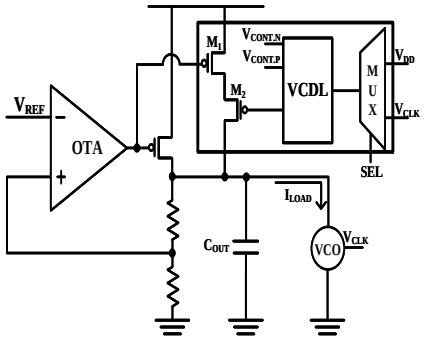
transistor and voltage-controlled delay line (VCDL) while using a smaller load capacitor.

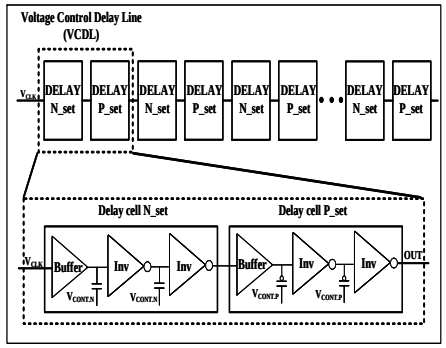
2.Implementation

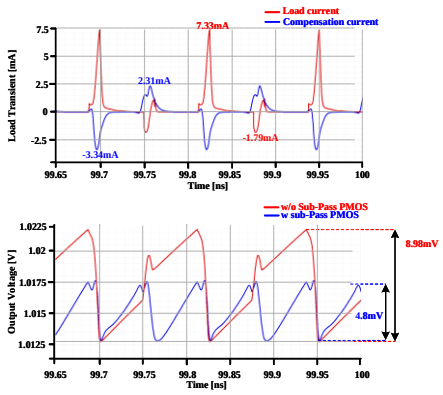
Fig. 1 depicts the complete block diagram of the proposed LDO regulator structure. The error amplifier is indicated as OTA and consists of a MUX for selecting the output (V_{DD} or V_{CLK}) depending on the *SEL* signal, a VCDL for timing alignment, M1 and M2 sub-pass transistors to provide compensatory current flow.

The V_{CLK} signal produced by the VCO is directed to one of the two input terminals of the MUX. If the LDO regulator is in a steady state, the MUX selects the V_{CLK} output through the *SEL* signal. The V_{CLK} signal, which is the output of the MUX, is then fed into the input of the VCDL. As shown in the comprehensive VCDL diagram in Fig. 2, the delay can be adjusted using a capacitor controlled by the control voltages ($V_{CONT,N}$, $V_{CONT,P}$). Furthermore, this delay can be manipulated to adjust one period of V_{CLK}. In the case of V_{CLK}, since it becomes a consistent clock signal when the VCO frequency is locked, adjusting one period through the VCDL enables synchronization of the output signals of V_{CLK} and VCDL at all timings.

The synchronized clock signal is then directed to the gate input of M2. M1 utilizes the output voltage of the OTA as feedback to maintain a consistent source voltage. Therefore, M2 guarantees a steady compensatory current flow. Ultimately, the timing diagram for the proposed structure is presented in Fig.







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